

Compal Confidential

UMA M/B Schematics Document Haswell with DDRIII + Lynx Point PCH

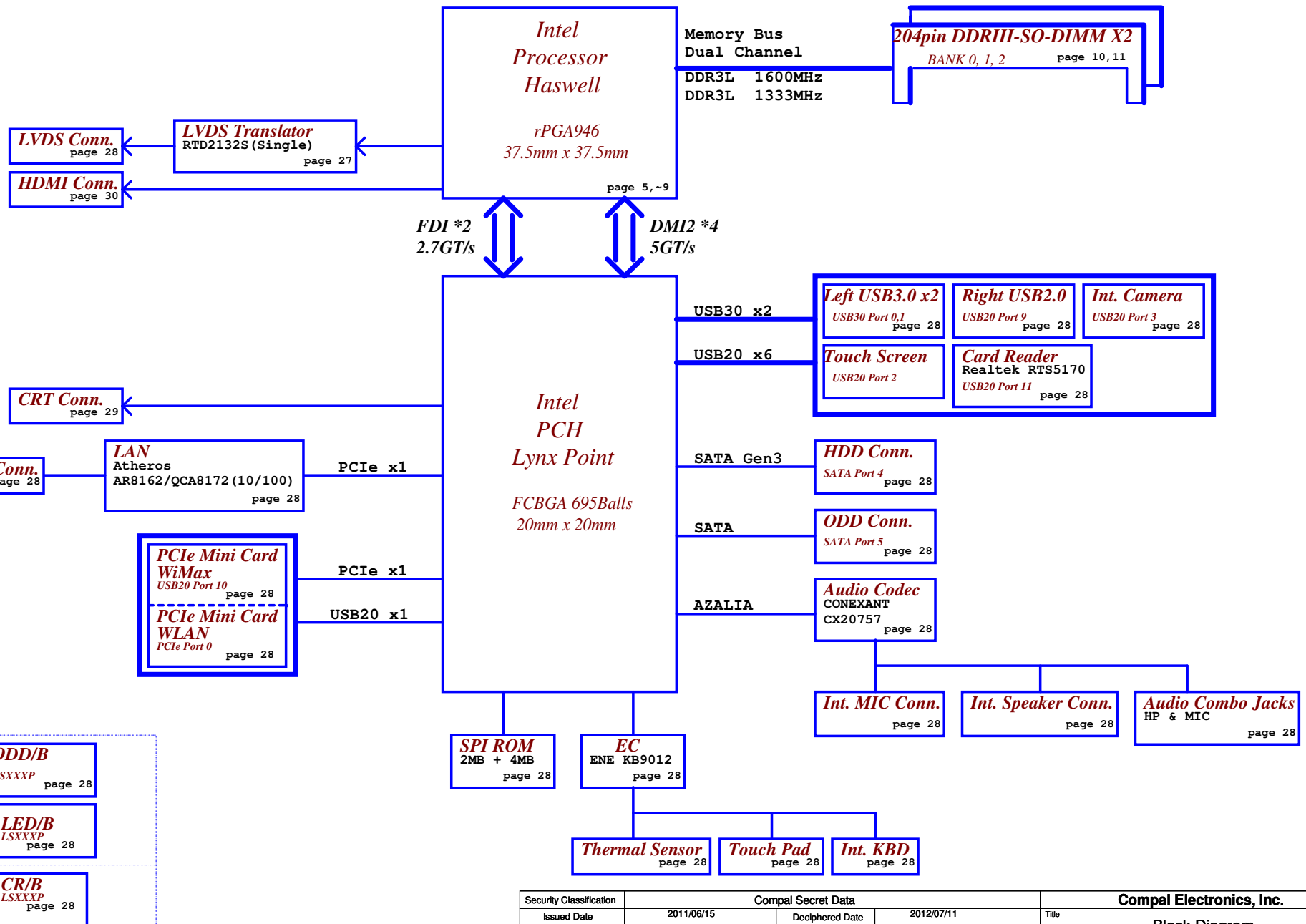
2012-10-03

LA-9642P

REV: 0.1

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Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	Cover Page
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Shark Bay



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Voltage Rails				
power plane	+B	+5VALW +3VALW	+1.35V	+5VS +3VS
				+VCC_CORE +VGA_CORE +1.5VS +0.675VS +1.05VS
State				
S0	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

Address

EC SM Bus1 address

EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Thermal Sensor F75303M	1001_101xb

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

NV-GPU SM Bus address

Device	Address
Internal thermal sensor	1001 111Xb (0x9E)

SMBUS Control Table									
	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH	RTD2132
SMB_EC_CK1	KB9012	✗	✓	✗	✗	✗	✗	✗	✗
SMB_EC_DA1	+3VALW		+3VALW						
SMB_EC_CK2	KB9012	✗	✗	✗	✗	✗	✗	✓	✓
SMB_EC_DA2	+3VALW							+3VS	+3VS
SMBCLK	PCH	✗	✗	✗	✓	✓	✗	✗	✗
SMBDATA	+3VALW				+3VS	+3VS			
SML0CLK	PCH	✗	✗	✗	✗	✗	✗	✗	✗
SML0DATA	+3VALW								
SML1CLK	PCH	✓	✗	✓	✗	✗	✓	✗	✓
SML1DATA	+3VALW	+3VS		+3VS			+3VS		+3VS

BOARD ID Table	
Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

USB Port Table			
	USB 2.0	Port	3 External USB Port
EHCI1	UHCI0	0	Left USB3.0
		1	Left USB3.0
	UHCI1	2	Touch screen
		3	Camera
	UHCI2	4	
		5	
	UHCI3	6	
7			
EHCI2	UHCI4	8	
		9	Right USB2.0
	UHCI5	10	WLAN
		11	Card reader
	UHCI6	12	
		13	

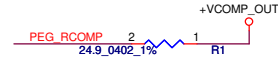
STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Vcc	3.3V +/- 5%	Board ID / SKU ID Table for AD channel					
Ra/Rc/Re	100K +/- 5%						
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max	Porject	Phase	
0	0	0 V	0 V	0 V	G-series	MP	
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	G-series	PVT	
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	G-series	DVT	
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	G-series	EVT	
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	Y-series	EVT	
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	Y-series	DVT	
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	Y-series	PVT	
7	NC	2.500 V	3.300 V	3.300 V	Y-series	MP	

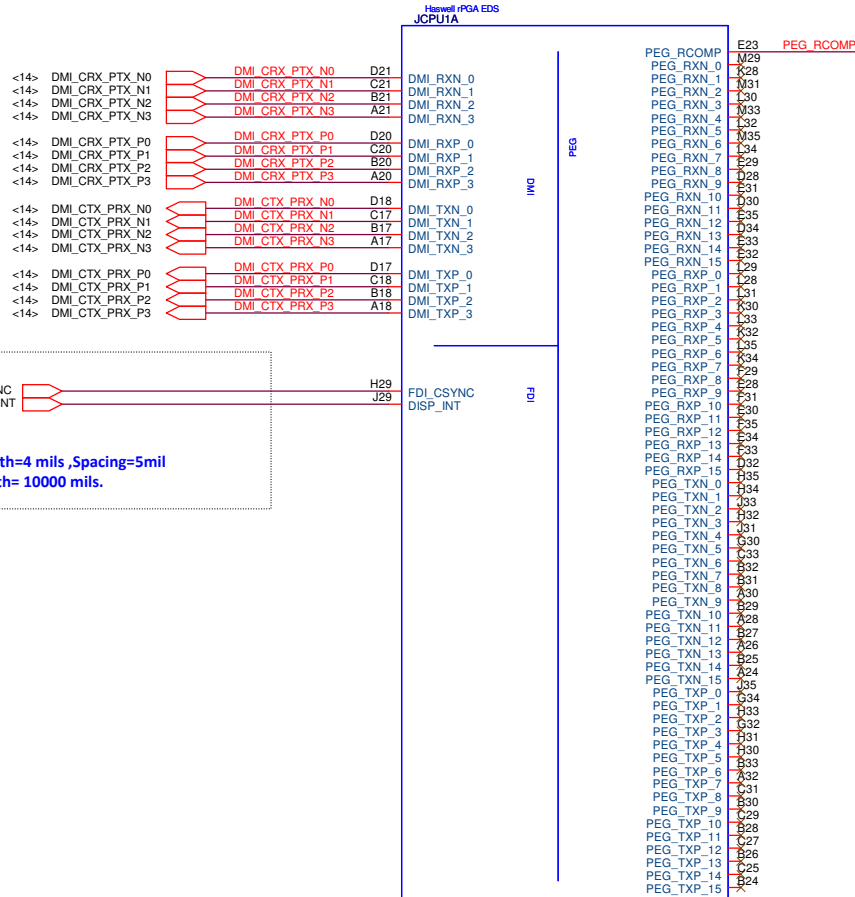
BOM Structure Table	
BTO Item	BOM Structure
HDMI	HDMI@
Connector	ME@
45 LEVEL	45@
10/100 LAN	
LAN LDO Mode	LDO@
LAN Switch mode	SWR@
Camera	CMOS@
For QIWG5 (14")	14@
For QIWG6 (15")	15@
Unpop	@

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PCB LA9641

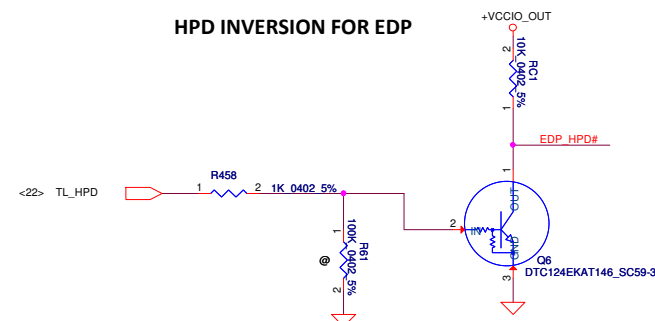
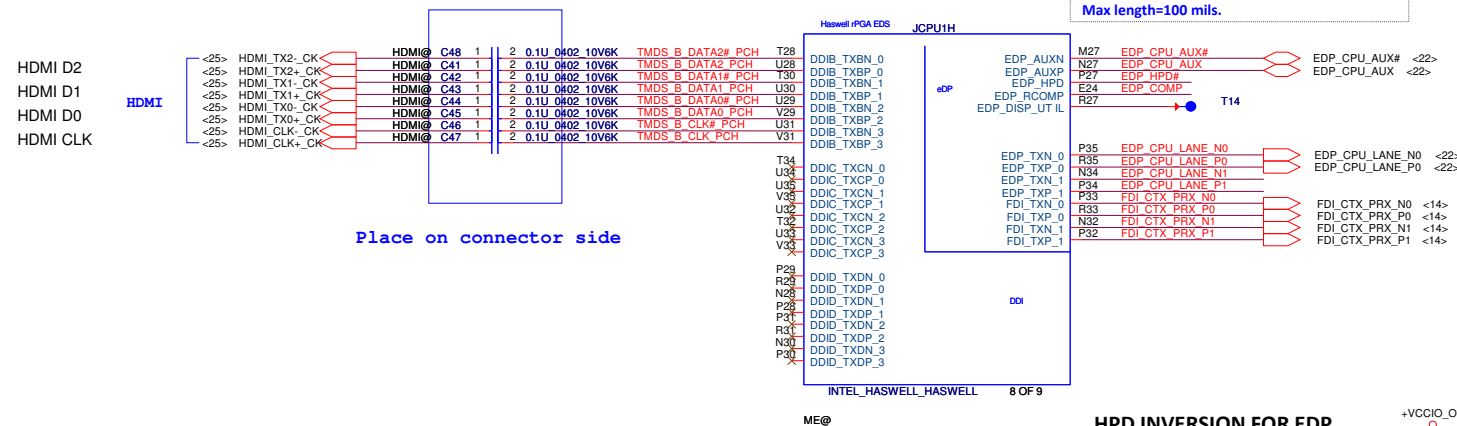
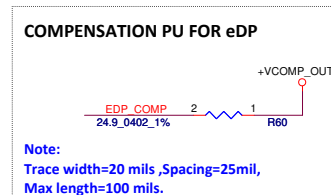


Note:
Trace width=12 mils ,Spacing=15mils
Max length= 400 mils.



INTEL_HASWELL_HASWELL 1 OF 9
ME@

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Issued Date				2011/06/15		Deciphered Date		2012/07/11		PROCESSOR(1/7) DMI,FDI,PEG	
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HPD is a active high signal from device. The HPD processor input is a low voltage active signal.

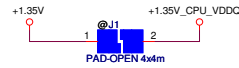
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Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	LA-9641P
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A schematic diagram showing a resistor labeled R62 with a value of 1K_0402_1%. The resistor is connected between a pin labeled CFG2 and a ground symbol. The connection points are labeled 1 and 2.

A circuit diagram showing a 1k resistor labeled R63. One terminal of the resistor is connected to a signal line labeled CFG4. The other terminal is connected to a ground symbol, represented by a triangle pointing downwards. The resistor is labeled with its value 1K_0402_1%.

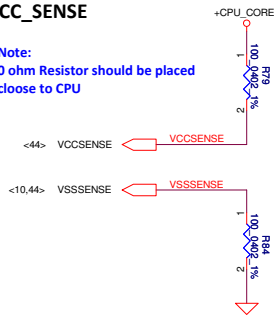
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Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	
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+1.35V_CPU_VDDQ Source

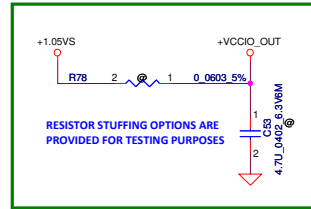
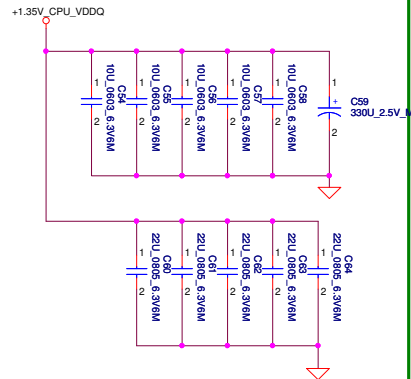


VCC_SENSE

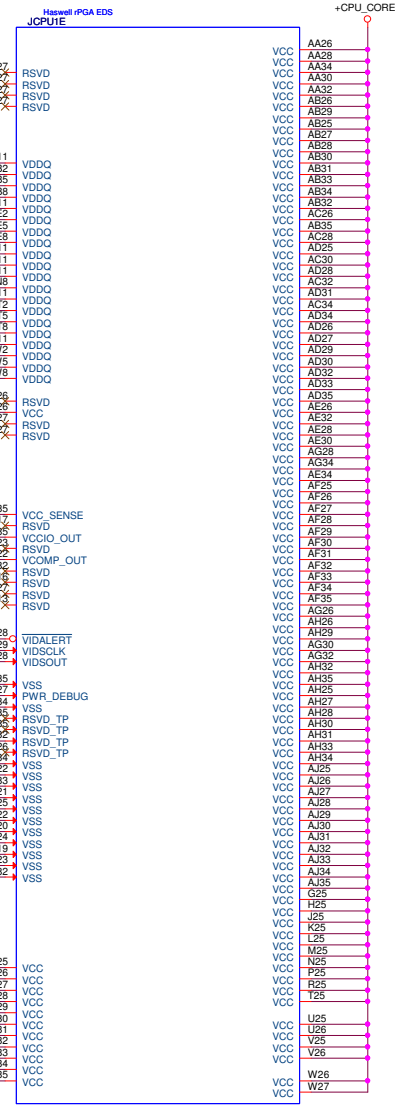
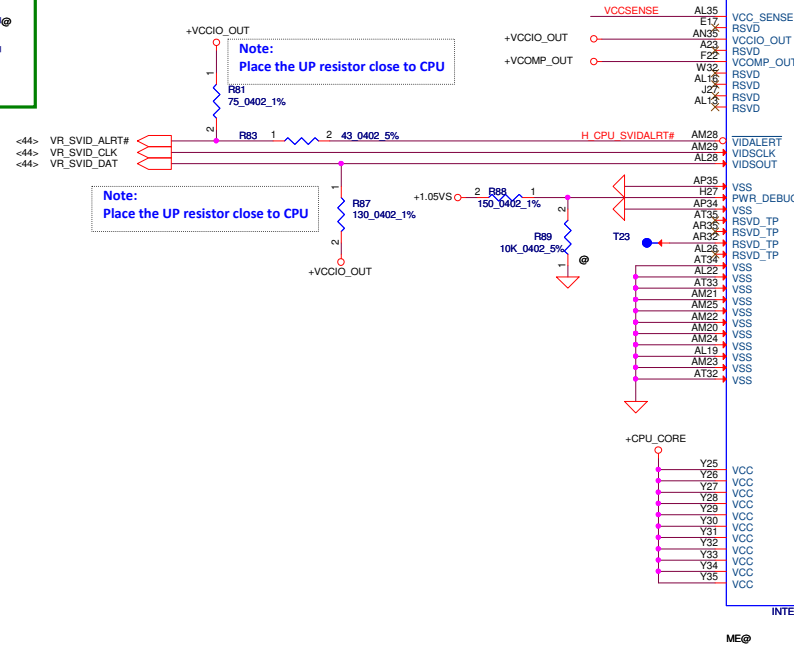
Note:
0 ohm Resistor should be placed
close to CPU



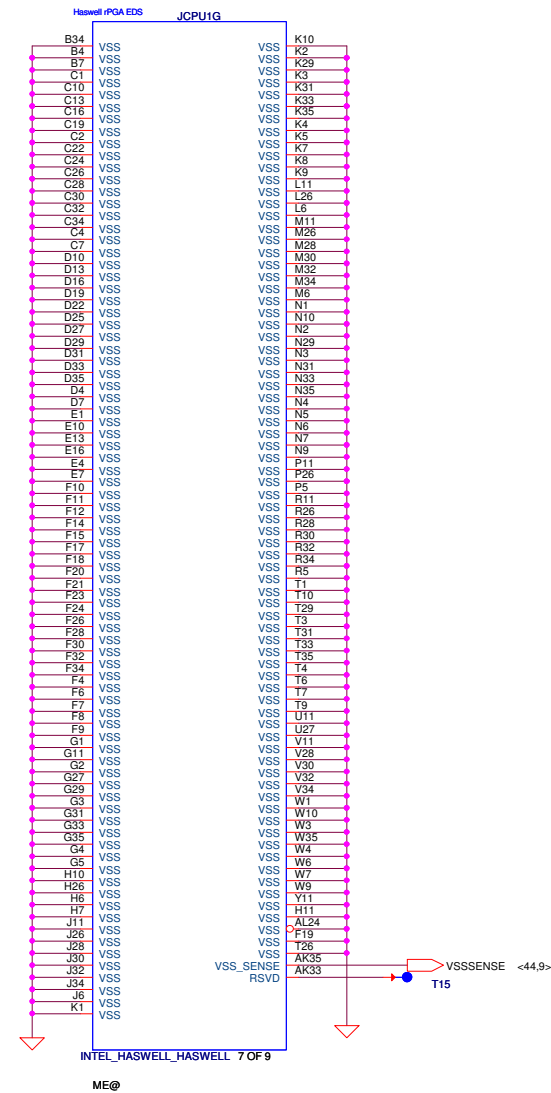
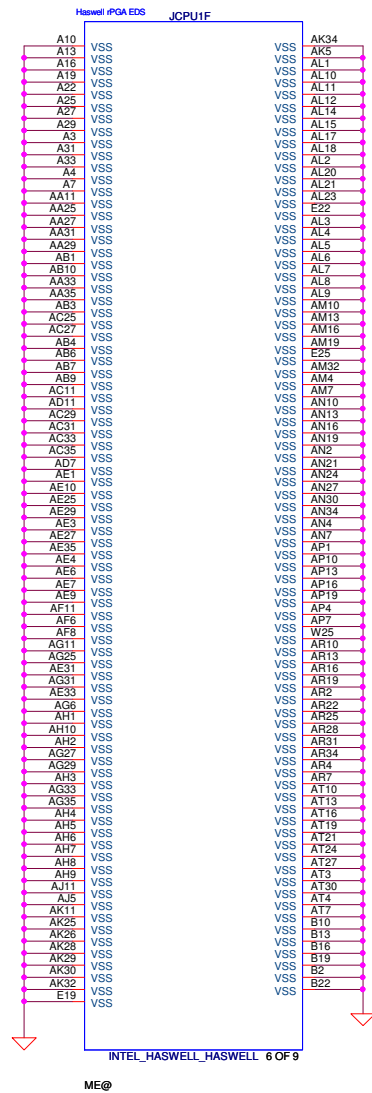
VDDQ DECOUPLING



RESISTOR STUFFING OPTIONS ARE
PROVIDED FOR TESTING PURPOSES

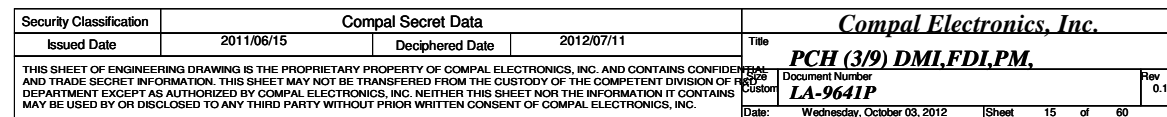
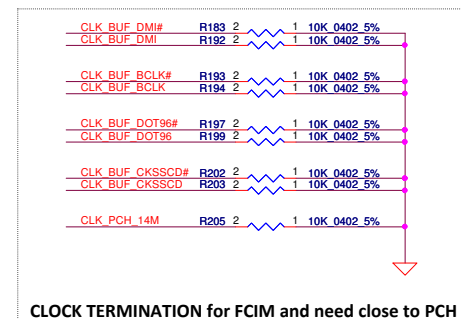


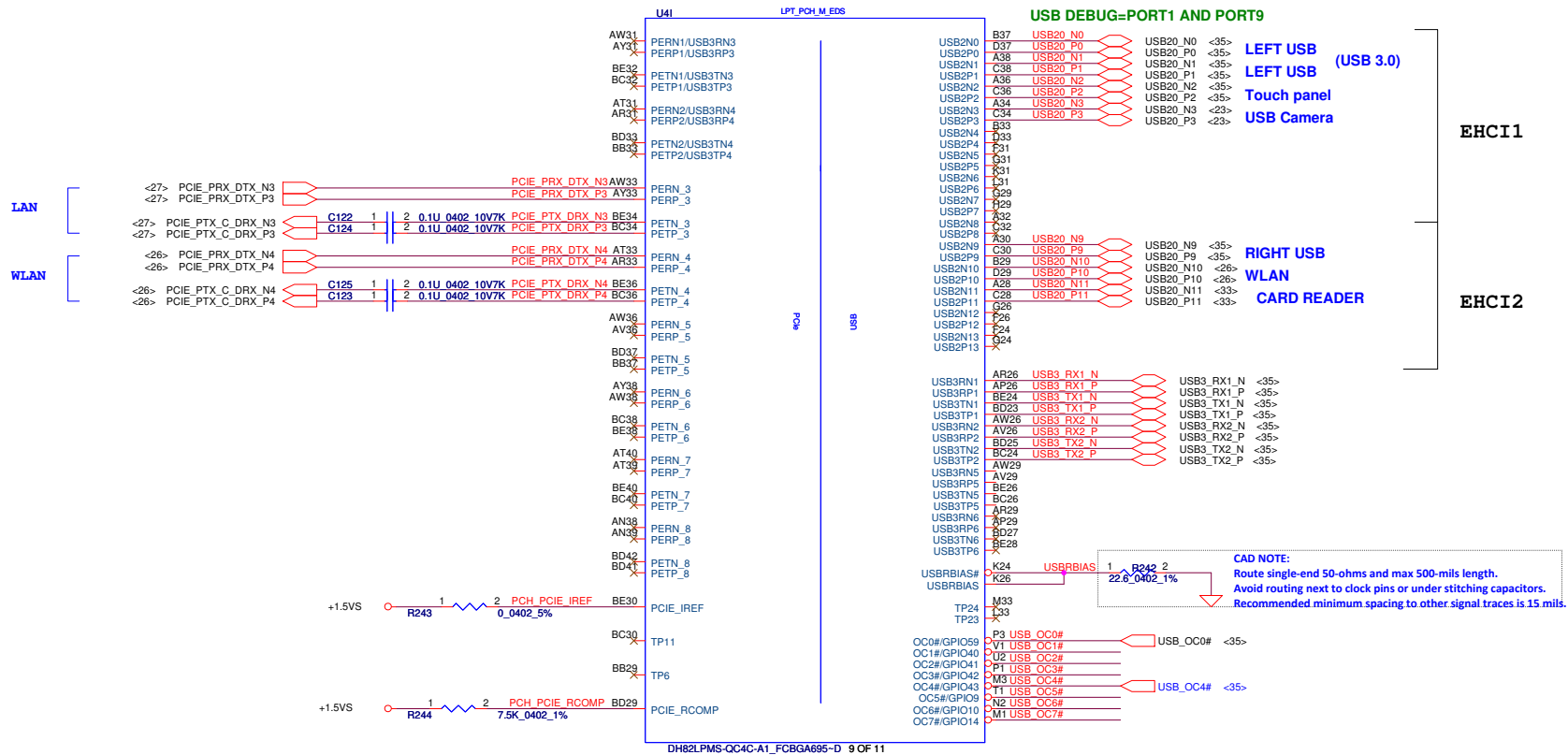
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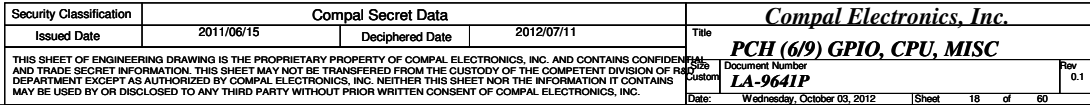
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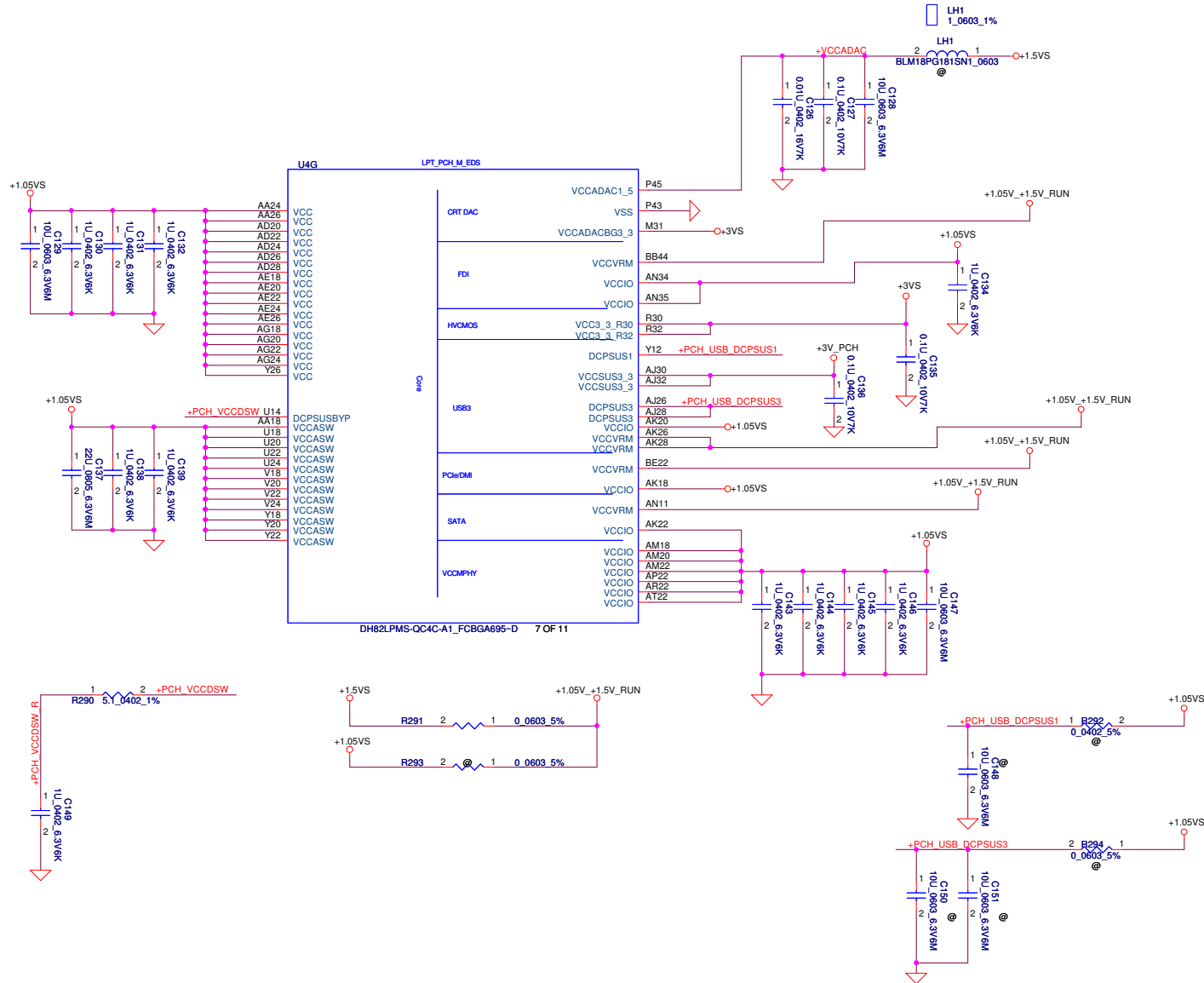




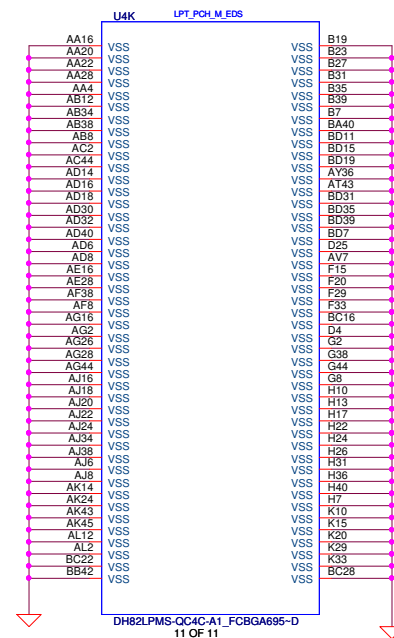
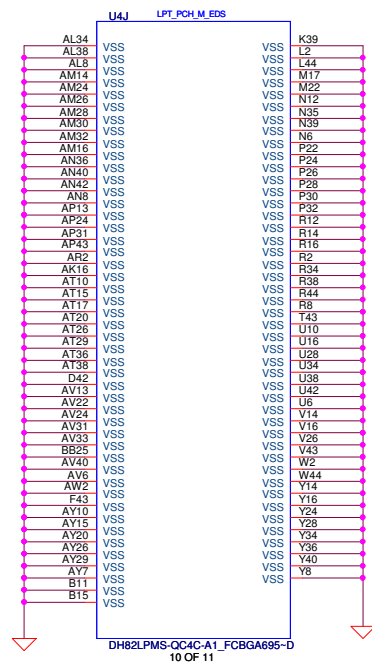


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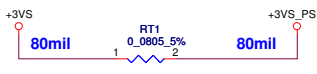




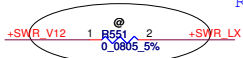
PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCDAC1_5	1.5V	0.070 A
VCCDAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A



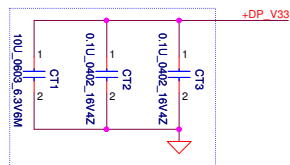
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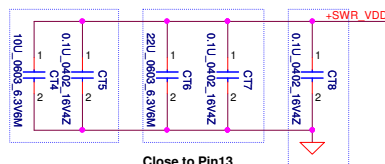
RTD2132R LDO MODE



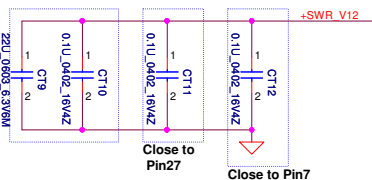
Close to Pin3



Close to L87



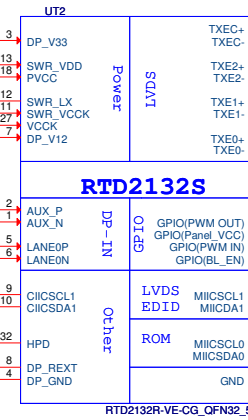
Close to L29



<7> EDP_CPU_AUX
<7> EDP_CPU_AUX#
<7> EDP_CPU_LANE_P0
<7> EDP_CPU_LANE_N0

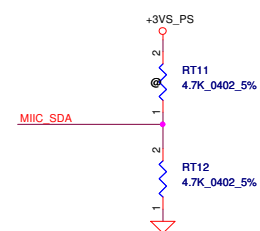
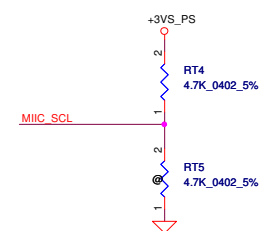
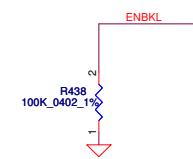
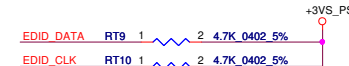
C190 1 2 0.1U 0402 10V6K EDP_CPU_AUX_R
C191 1 2 0.1U 0402 10V6K EDP_CPU_AUX#_R
C192 1 2 0.1U 0402 10V6K EDP_CPU_LANE_P0_R
C193 1 2 0.1U 0402 10V6K EDP_CPU_LANE_N0_R

<16,29,32> EC_SMB_CK2
<16,29,32> EC_SMB_DA2
<7> TL_HPD



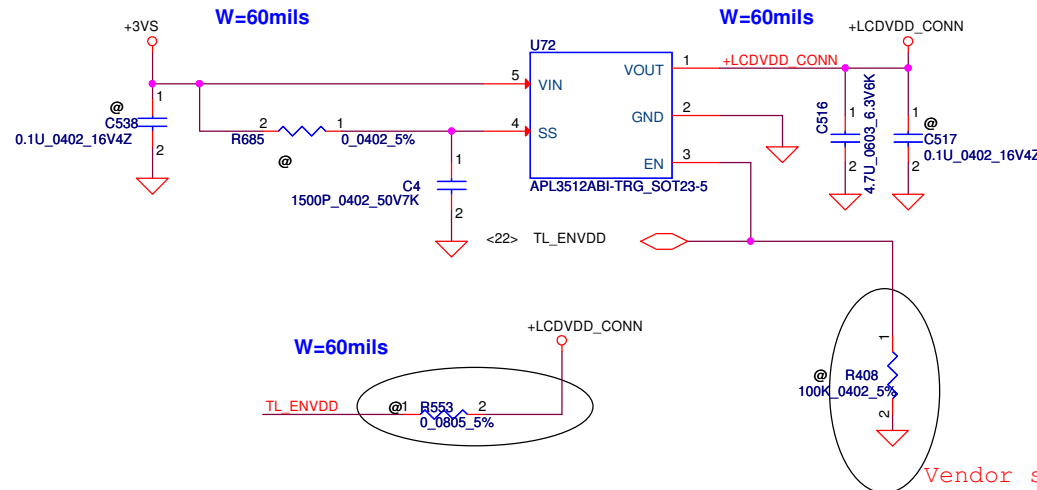
TL_ENVDD need 40 mil if use for LVDS power on R version

ADD TP on trace or via

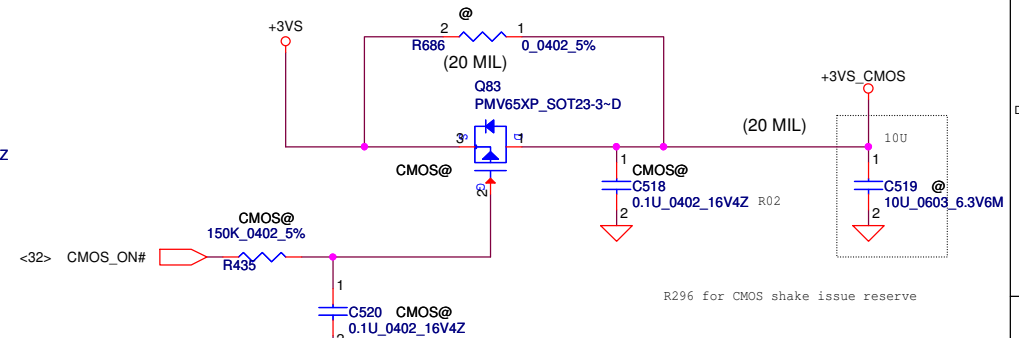


MIIC_SCL \ MIIC_SDA	MIIC_SDA	
	0	1
0	X	EC CODE
1	Internal ROM	EEPROM

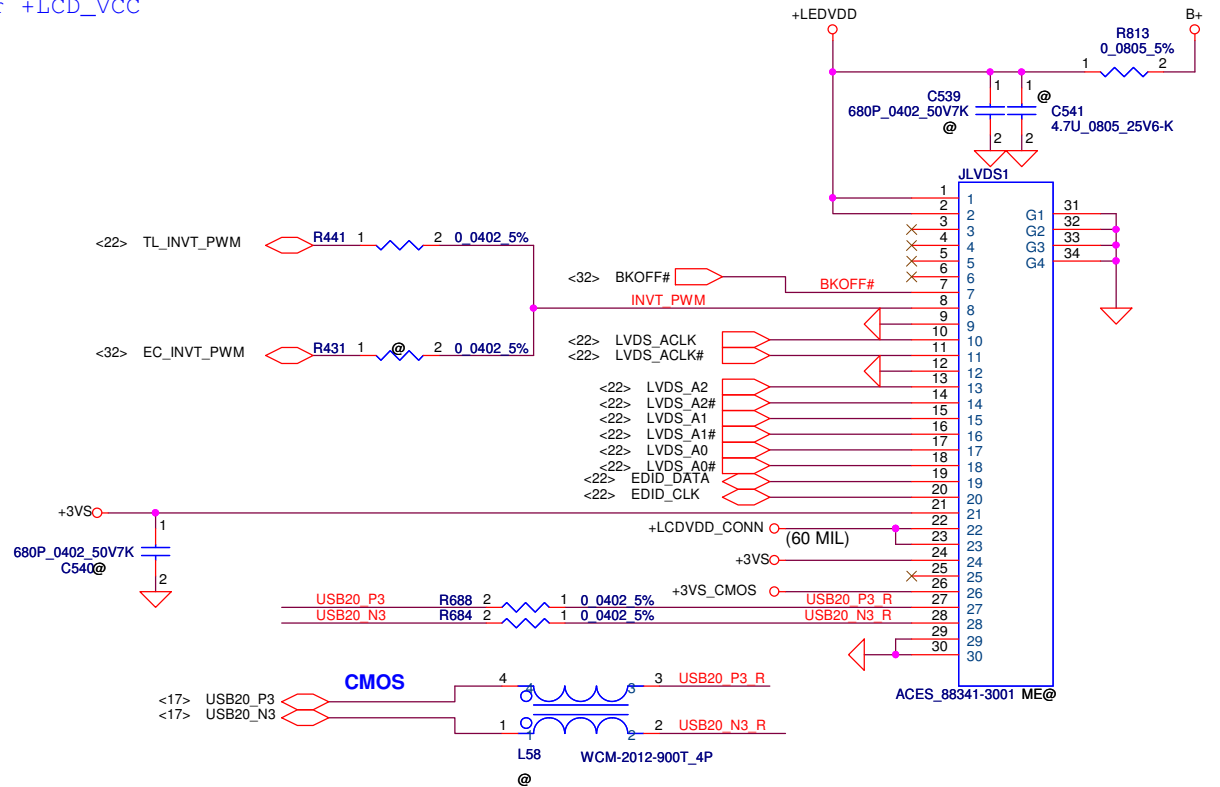
LCD POWER CIRCUIT



CMOS Camera

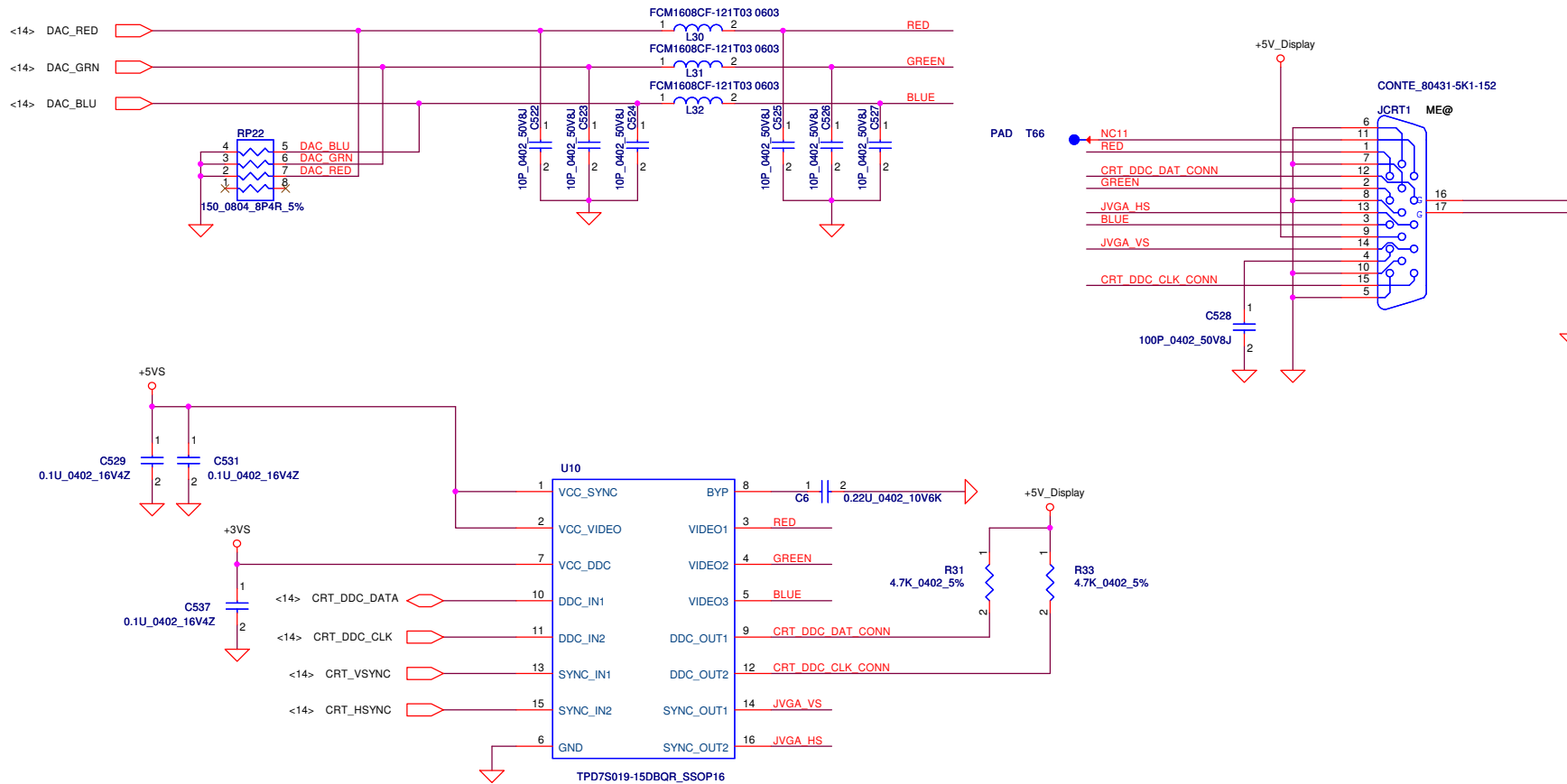


VGA LCD/PANEL BD. Conn.

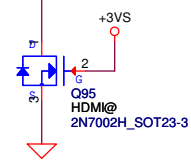
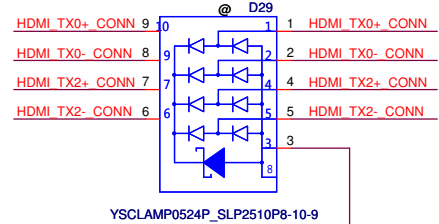
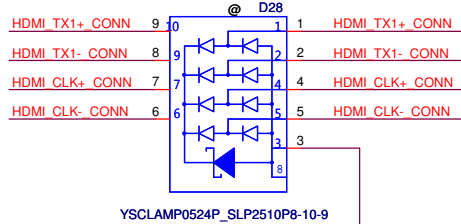
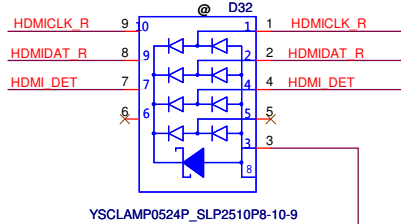
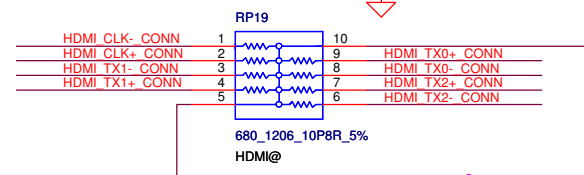
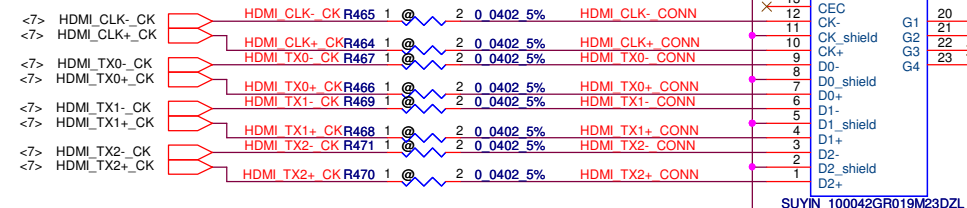
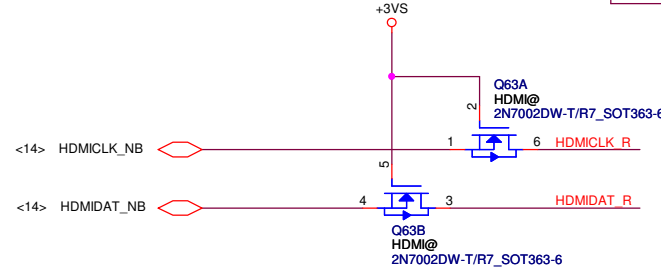
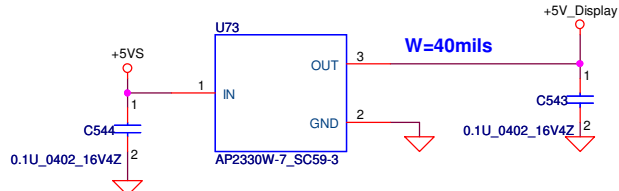
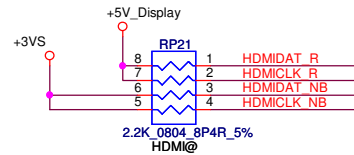
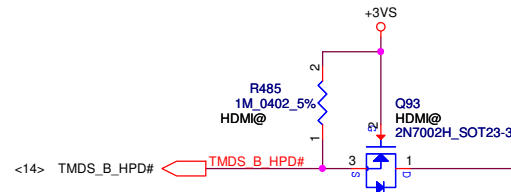
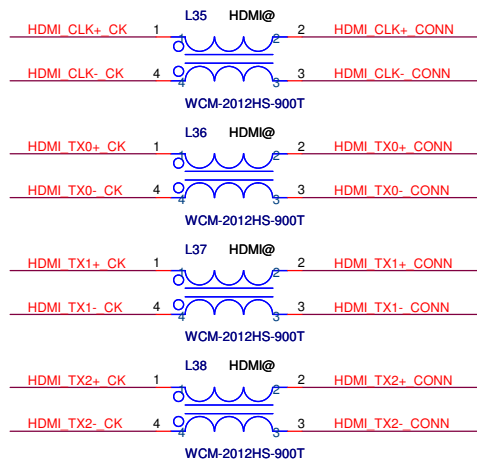


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Issued Date		2011/06/15	Deciphered Date	2012/07/11	Title		
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					Size	Document Number	Rev
					Custom	LA-9641P	2.0
Date:		Wednesday, October 03, 2012		Sheet	23	of 60	

CRT Connector

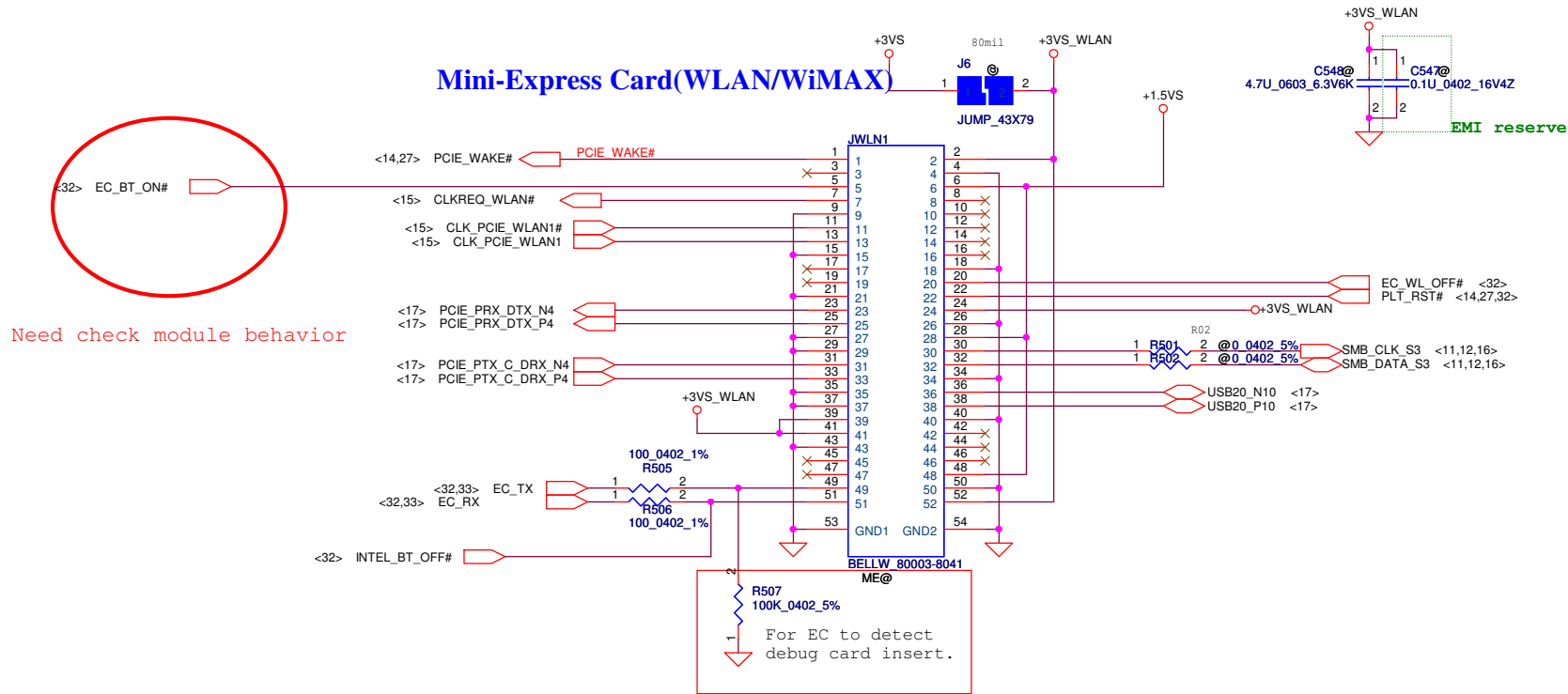


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Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	
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Size	Custom	Document Number	LA-9641P	Rev 2.0	
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				LA-9641P	
				Date: Wednesday, October 03, 2012	Sheet 25 of 60

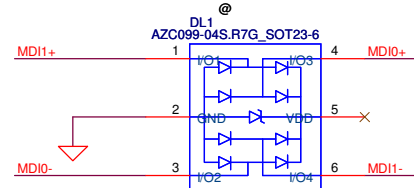
Mini-Express Card for WLAN/WiMAX(Half)



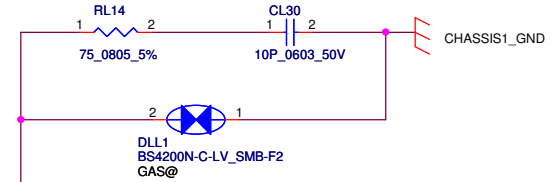
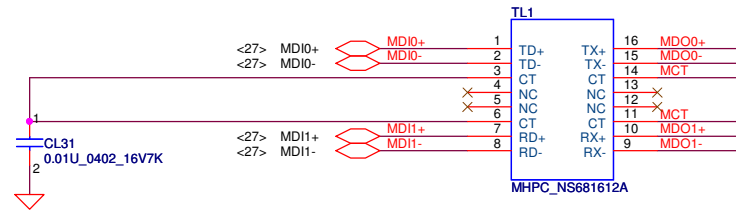
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	Mini-Card/NEW Card/SIM
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				Date	Wednesday, October 03, 2012
				Sheet	26 of 60
				Rev	2.0

DL1
1'S PN:SC300001G00
2'S PN:SC300002E00

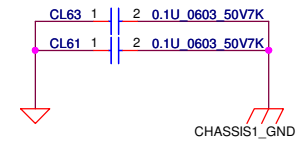
Place Close to TL1



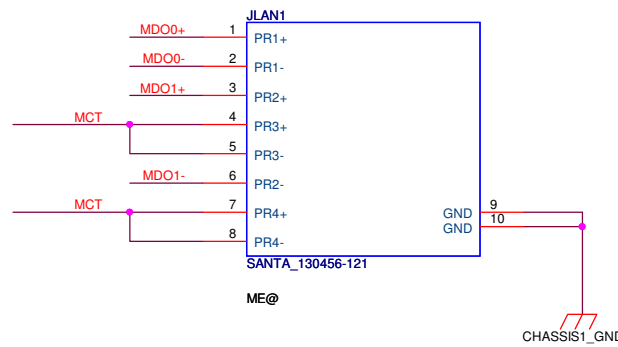
Reserve gas tube for EMI go rural solution



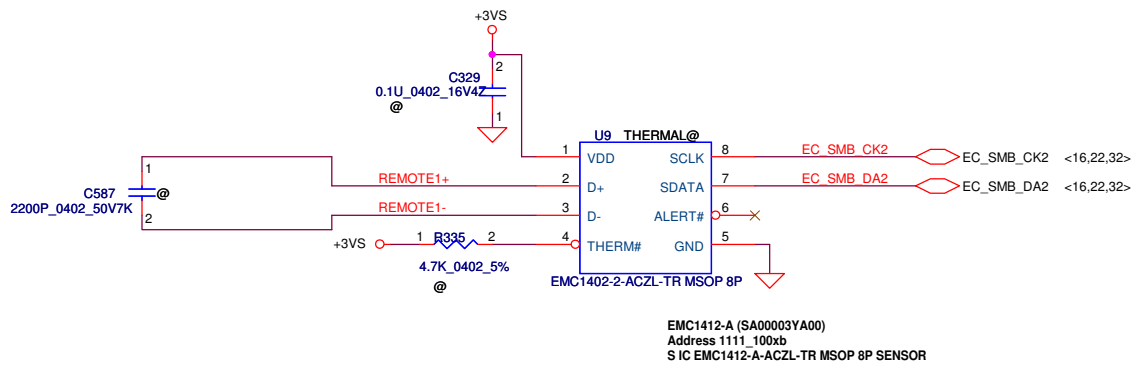
Place Close to TL1



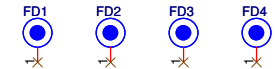
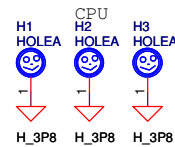
Need check Symbol



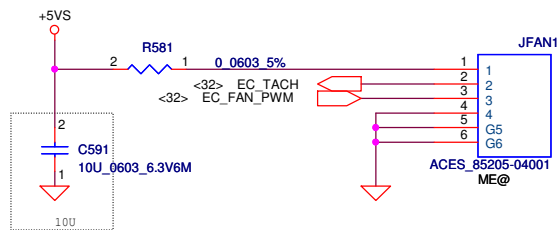
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	LAN_Transformer
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REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"



FAN1 Conn

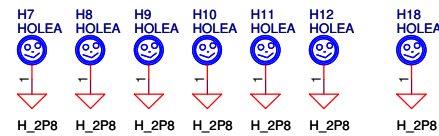


A

B

M/B 橢圓孔

M/B 圓孔



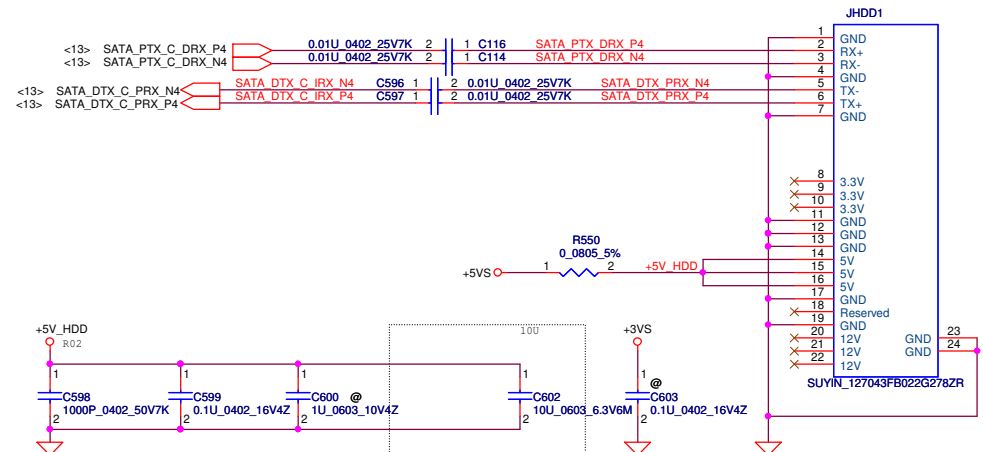
2P8 * 7 pcd

D

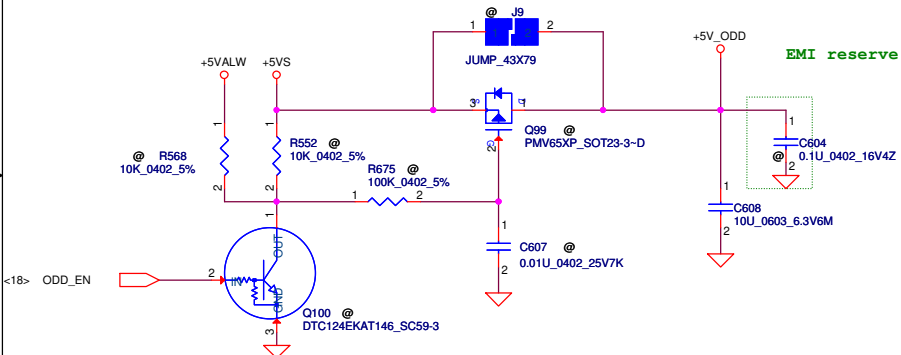
E

Security Classification	Compal Secret Data			Compal Electronics, Ltd.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title Fintek-Thermal IC/FAN/screw	
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				LA-9641P	2.0
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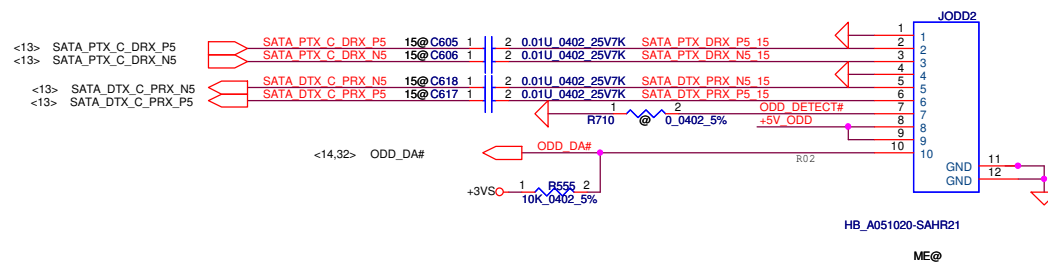
SATA HDD Conn.



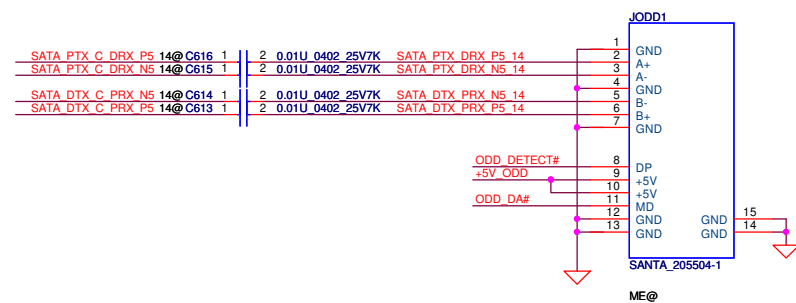
ODD Power Control



FOR 15" SATA ODD FFC Conn.



FOR 14" SATA ODD Conn.



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Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	HDD/ODD/BT Connector	
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CX20751
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).

Sense resistors must be
connected same power
that is used for VAUX_3.3

mount RA6 on the Jack Sense circuit
to configure Port-C for mono MIC.

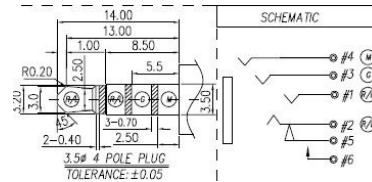
Don't support LINE_IN function
RA7 could be @

CA3 vendor suggest
change to 2.2U

AVDD_3.3 pins output of
internal LDO. NOT connect
to external supply.

Layout Note: Path from +5VS to LPWR_5.0
RPWR_5.0 must be very low
resistance (<0.01 ohms)

Please bypass caps very close to device.



Check footprint

HGND, HGND 80mils

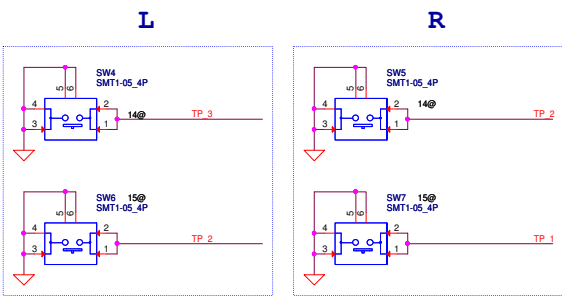
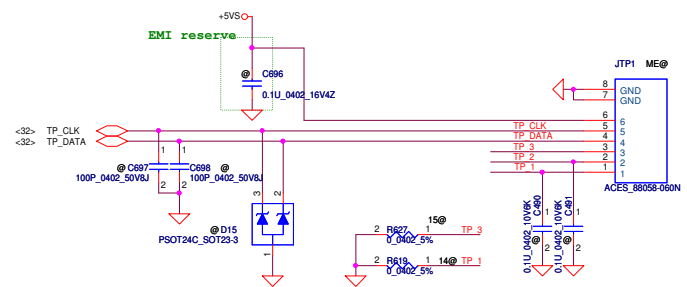
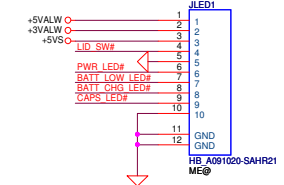
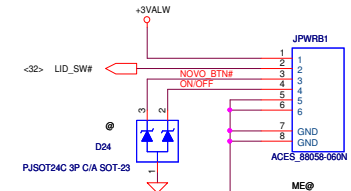
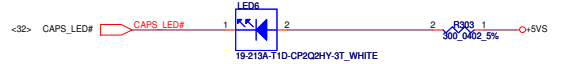
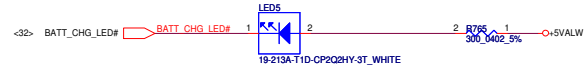
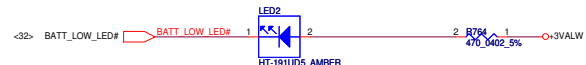
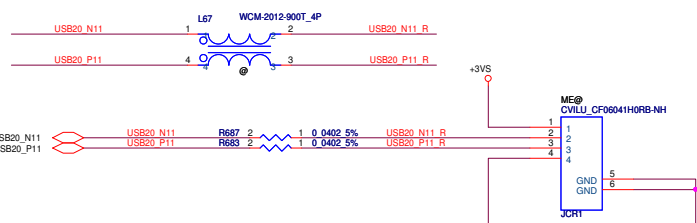
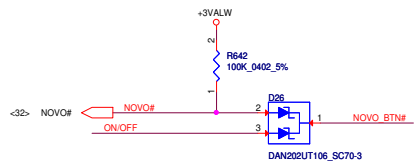
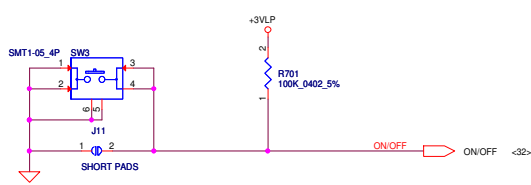
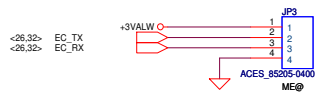
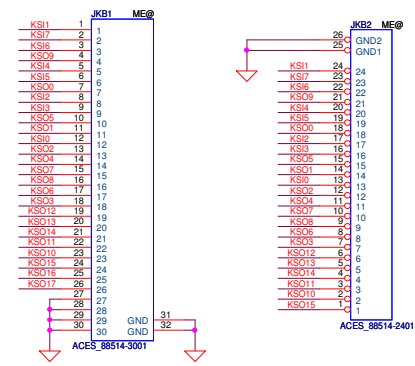
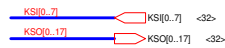
for Universal jack

wide 20MIL

vendor suggest
change to 1000p

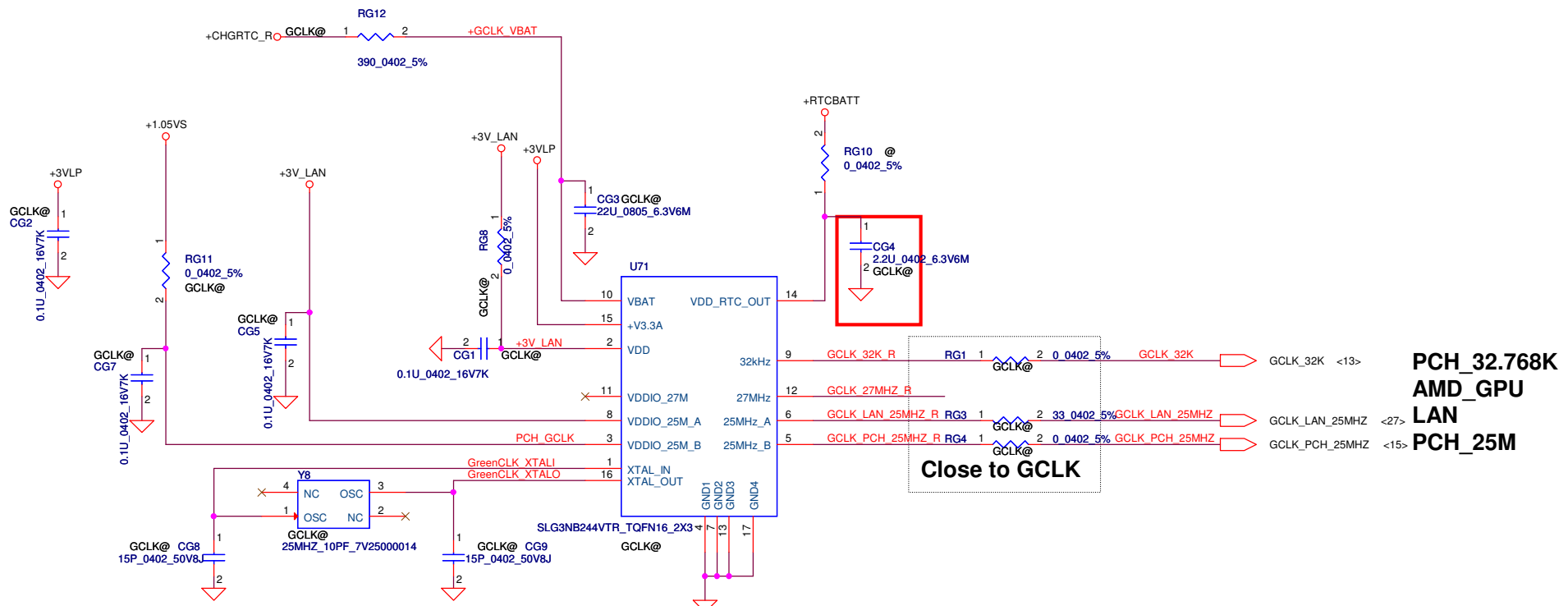
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	CX20751 Codec	
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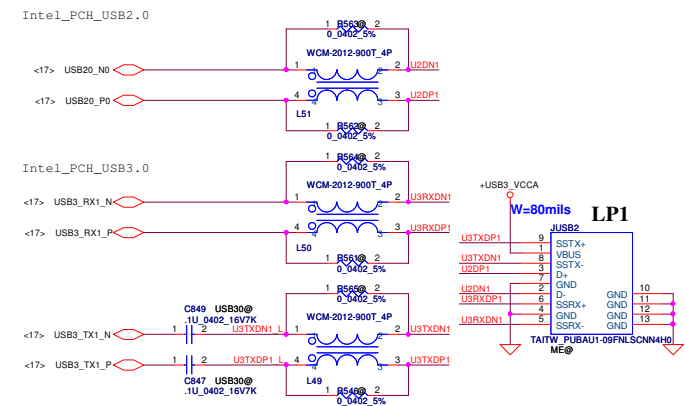
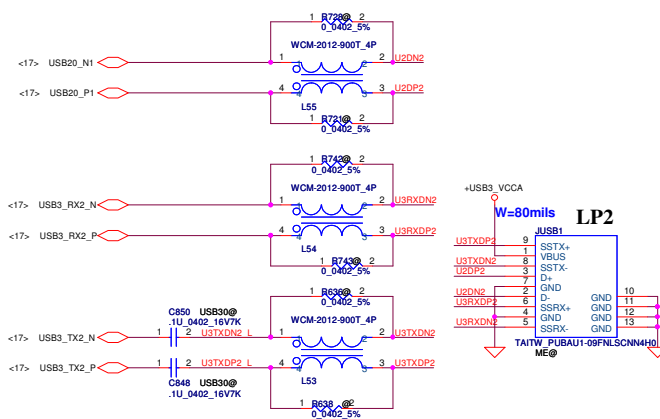
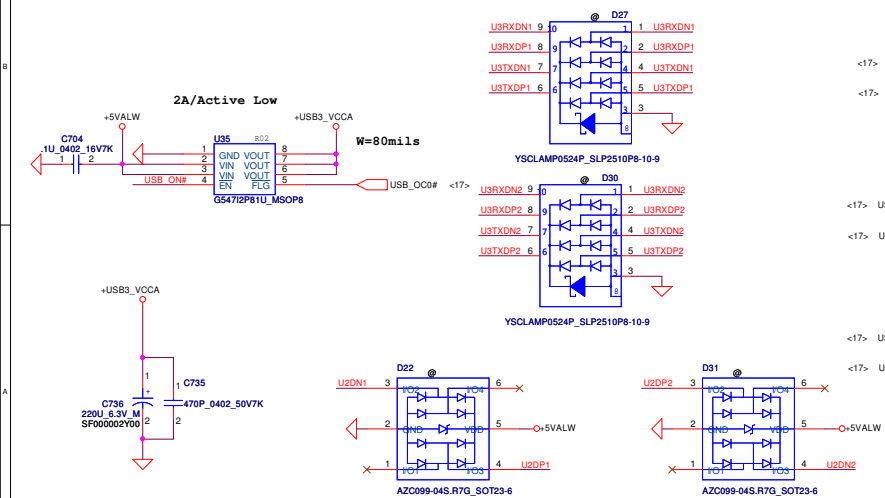
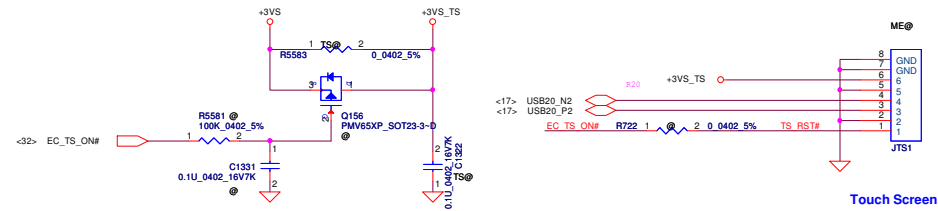
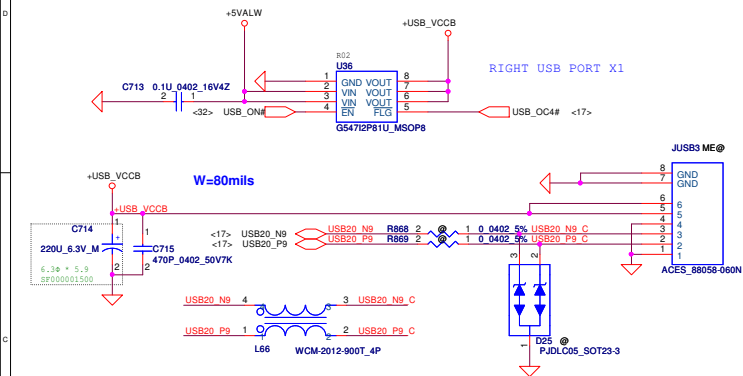
15"	14"
1 VCC	1 VCC
2 CLK	2 CLK
3 DAT	3 DAT
4 GND	4 L
5 L	5 R
6 R	6 GND

Green Clock

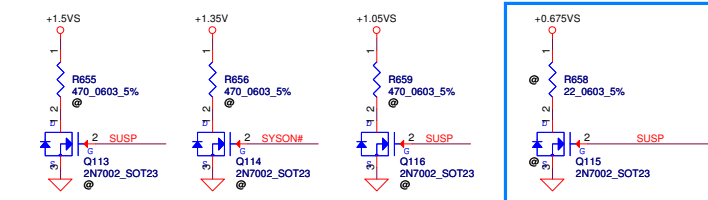
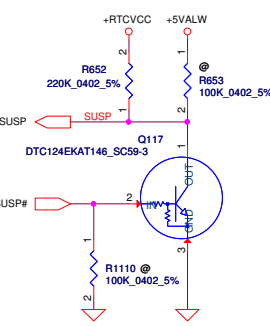
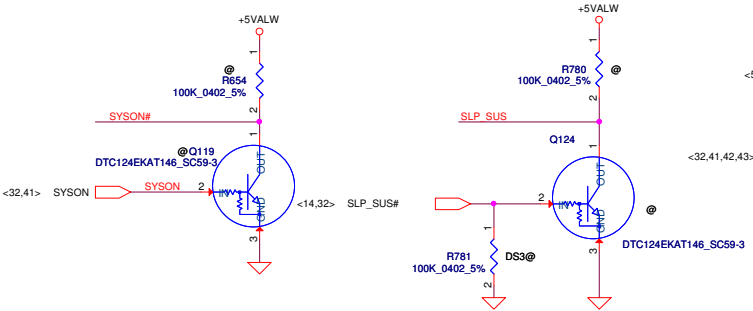
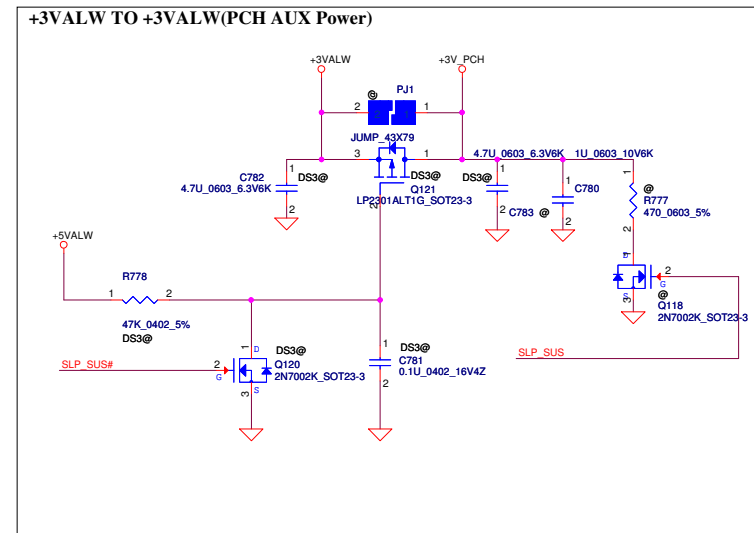
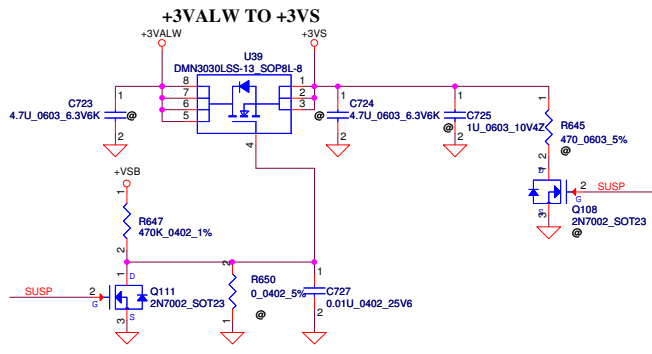
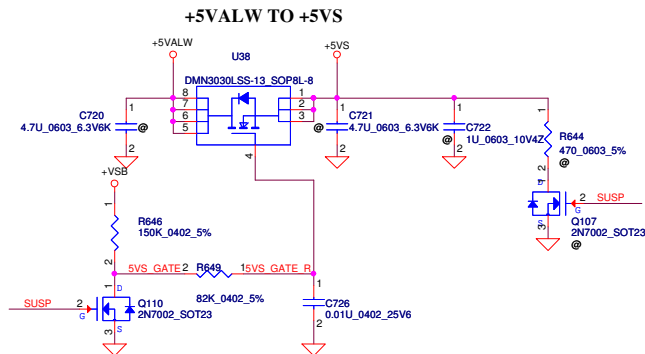


Reserved for Swing Level adjustment
(Close GCLK side)

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				Date: Wednesday, October 03, 2012	Sheet 34 of 60

Right Ext.USB Conn.

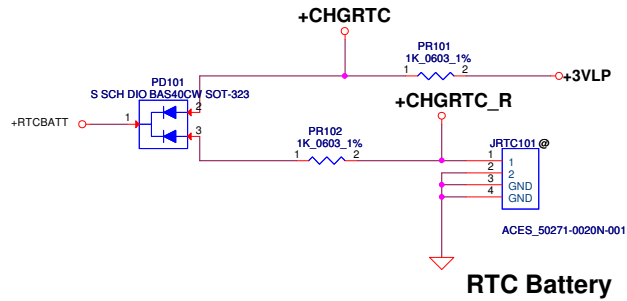
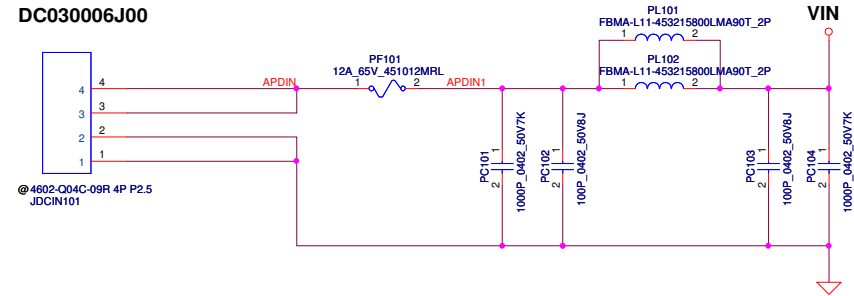
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Issued Date		Deciphered Date		2012/07/11	
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				Size	Document Number
				Date	Wednesday, October 03, 2012
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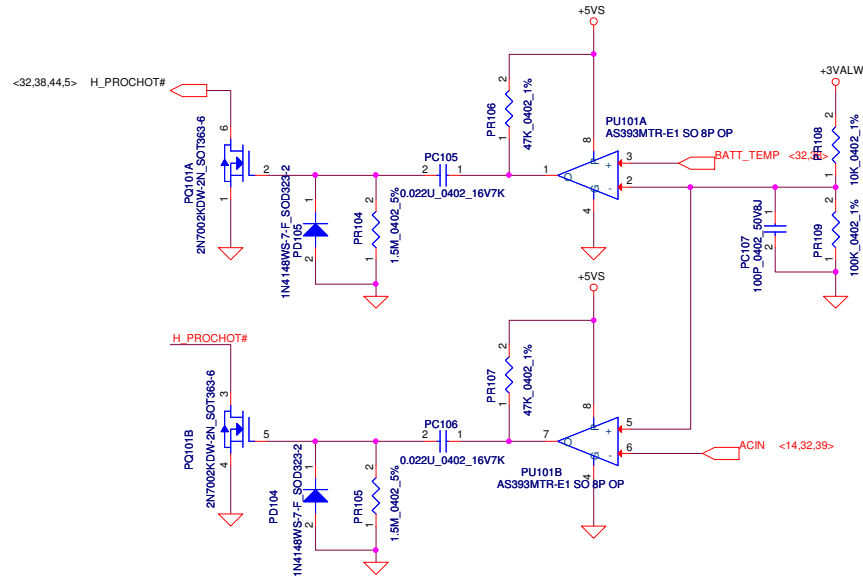
For Intel S3 Power Reduction.

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					Size	Document Number	Rev
					Custom	LA-9641P	2.0
					Date:	Wednesday, October 03, 2012	Sheet

DC030006J00



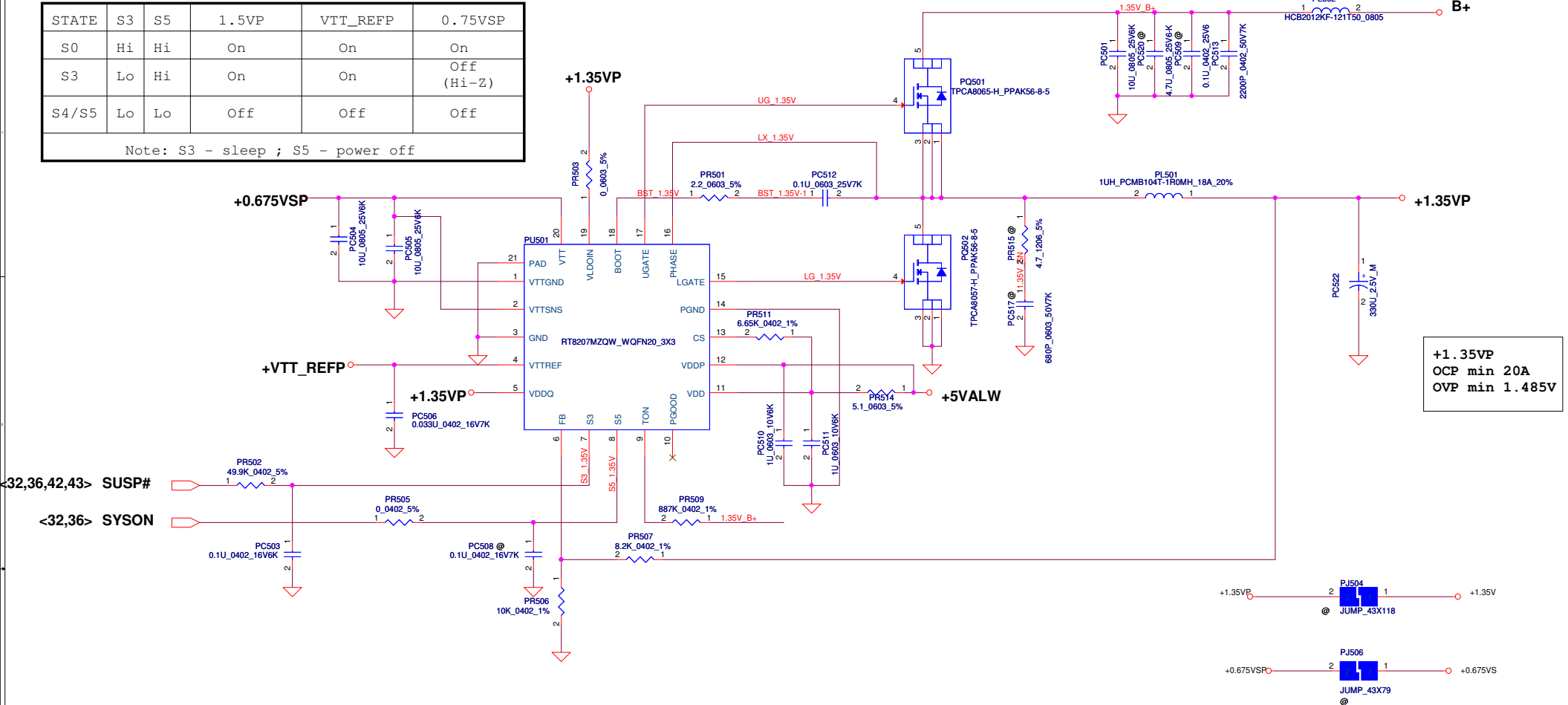
RTC Battery

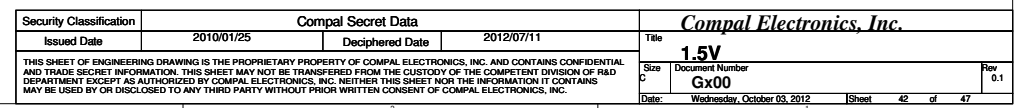
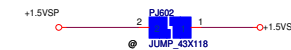


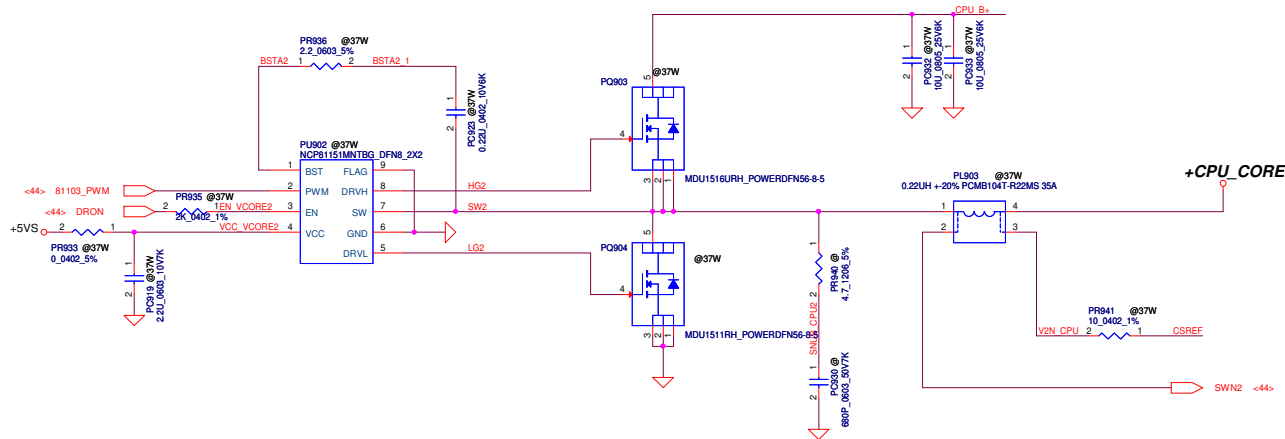
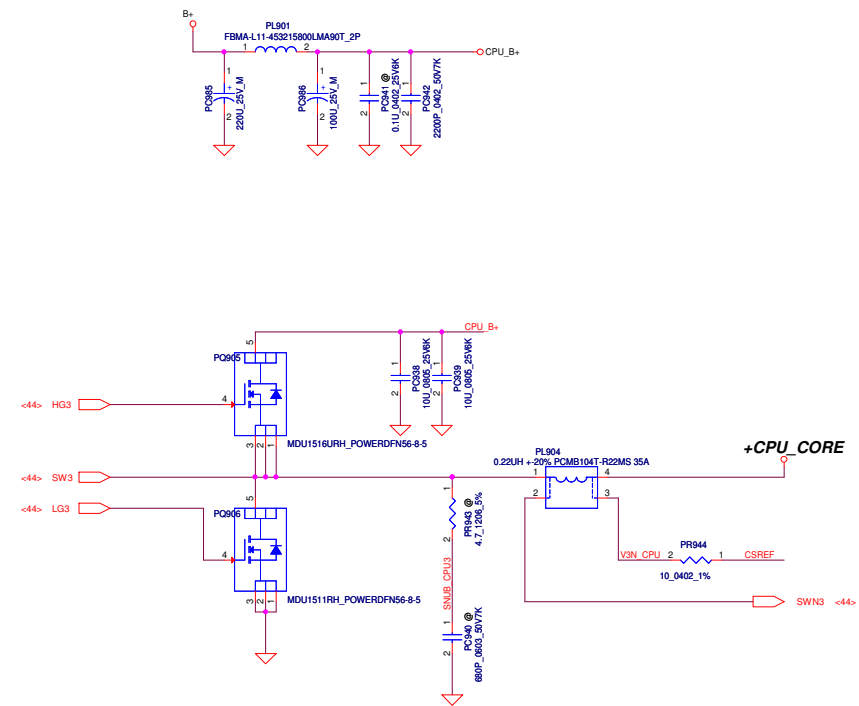
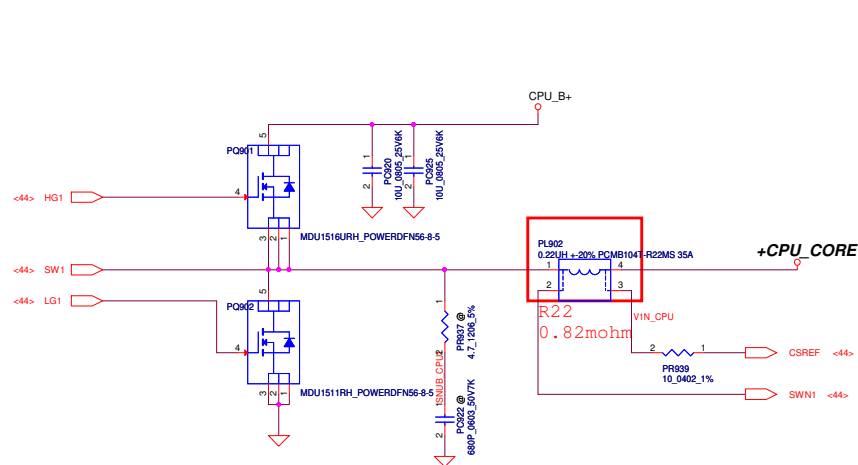
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2010/01/25	Deciphered Date	2012/07/11	Title	PWR DCIN / RTC Battery
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				Sheet	37 of 47
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STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Note: S3 - sleep ; S5 - power off

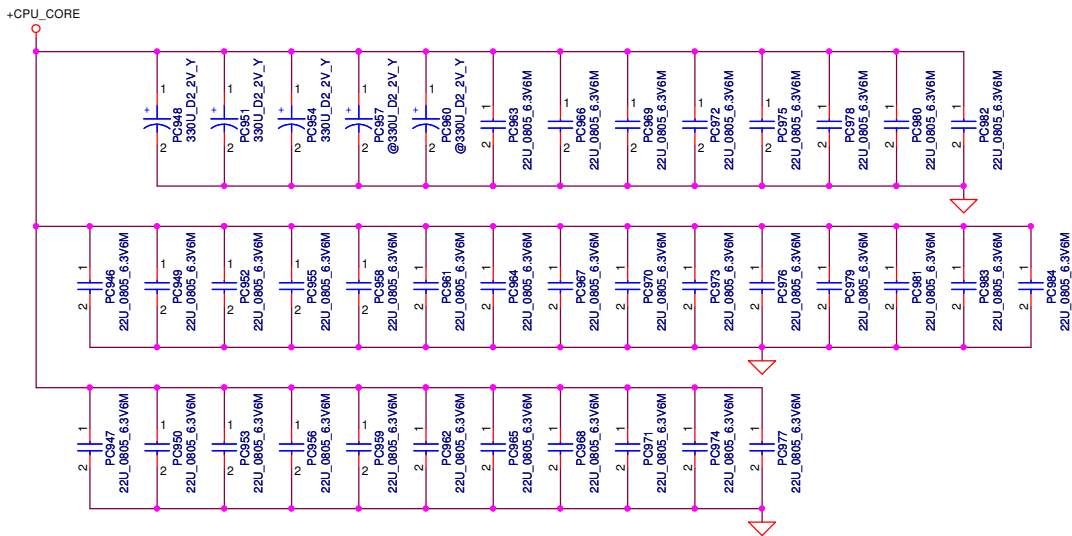






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+CPU_CORE 3 X 330u/9m (47W) 2X330u/9m (37W)
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